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Effects of High-K Dielectric on the Performance Parameters of GNR-FETs

Md Akram Ahmad, Jitendra Kumar*

Department of Electronics Engineering, Indian Institute of Technology Dhanbad, 826004, Dhanbad, Jharkhand, India.

Abstract

This article examines the dielectric strength of the gate oxide and its impact on the performance of a field-effect transistor (FET) made with graphene nanoribbons (GNR). The study uses non-equilibrium Green's Function (NEGF) formalism and tight binding frameworks to analyze the device's transfer characteristics, ON-current (I_{ON}), OFF-current (I_{OFF}), current ON/OFF ratio (I_{ON}/I_{OFF}), transconductance (g_m) and transconductance generation factor (TGF). The results obtained by solving the NEGF and Poisson's equation self-consistently in NanoTCAD ViDES environment, show that the device's performance is heavily influenced by the dielectric strength.

Keywords: Graphene nanoribbon (GNR), Field-effect-transistor, non-equilibrium green's function (NEGF), High-k dielectric.

Full length article **Corresponding Author*, e-mail: akram14407@gmail.com

1. Introduction

In recent decades, there has been significant transistor scaling due to the need for integrated circuits to consume less power [1]. From one point of view, scaling can lead to advancements in power efficiency, speed, features, device cost, and the number of devices that can fit on a chip [2-3]. However, when the length of devices reaches the scale of tens of nanometers, certain unfavorable consequences emerge in the electrical properties of the device, such as threshold voltage roll-off, DIBL, an increase in leakage current, and subthreshold slope [4-7]. To address these negative impacts of scaling on short-channel devices, various techniques have been suggested by device experts and reporters, such as tunnel FET, FD-SOI MOSFET, FinFET, III-V compounds, GAA-FET, and alternative 2D materials like graphene [8-23].

Graphene, which has a lattice structure resembling a honeycomb and exists in two dimensions, was developed for use in RF applications because of its high carrier mobility, concentration, velocity, and thermal conductivity. However, in order to utilize graphene in electronic applications, it is necessary to create a bandgap. As a result, narrow strips of graphene called graphene nanoribbons (GNRs) are created for use in electronic applications, and the GNR-based field-effect transistor (FET) is known as the GNR-FET. Several methods exist to enhance the electrical capabilities of a typical GNR-FET device [23].

Techniques such as modifying the gate material's work function, adjusting channel doping, and implementing voltage difference engineering are some methods that can be used to improve the electrical performance of a GNR-FET device [24-30]. The change in the gate dielectric method is considered the most fascinating of all these ideas. Several research groups have achieved encouraging outcomes in their studies of high-k dielectric materials, including hafnium silicate, lanthanum oxide, titanium dioxide, yttrium oxide, aluminum oxide, hafnium oxide, and zirconium oxide. These materials possess a high dielectric constant and are utilized in various applications, such as microelectronics and energy storage. The performance of these materials depends significantly on their composition and structure, and researchers are striving to optimize their properties to suit specific applications.

The continuous exploration and development of high-k dielectric materials hold the potential to transform many industries, ranging from electronics to renewable energy [31-37]. The main aim of this article is to investigate the impact of GNR-FET high-k gate dielectric on various aspects such as drive current, leakage current, and short channel effects. To conduct the simulation, the non-equilibrium Green's Function (NEGF) formalism has been utilized along with the self-consistent solution of two-dimensional (2D) Poisson-Schrödinger equations [38].

Apart from examining the short channel effects (SCEs), the AC performance parameters including transconductance and transconductance generation factor have been analyzed to gain a deeper understanding of the channel material.

2. Materials and methods

Fig. 1 depicts the simulated structure of a double-gated (DG) GNR-FET device. The device structure consists of an armchair graphene (A-GNR) channel material constructed from 12-dimer carbon atoms proportional to the device's width. The channel length (L_{ch}) is set to 10 nm, and the source/drain extension lengths (L_S,L_D) are individually patterned to a length of 10 nm. The source/drain regions have a donor-type doping concentration of 2.5 x 10^{13} cm^{-2}. The thickness of the top and bottom gate oxides is 2 nm. The drain is biased with a voltage of 0.5 V at 300 K. All simulations were performed using the non-equilibrium Green's function (NEGF) framework with the tight-binding approach-based atomistic device simulator NanoTCAD ViDES. In the NEGF method, the most crucial variable is the Green's function, $G(E) = [EI - H - \Sigma_S - \Sigma_D]^{-1}$, which is established using previous work. The drain current is determined using the Landauer formula [39]. Here, E, I, H, Σ_S and Σ_D indicates energy, identity matrix, Hamiltonian of the material, self-energy matrix for the source and drain terminals, respectively.

3. Results and Discussions

In order to meet the technological demands of the present and future, it is crucial to minimize the channel length as much as possible. However, reducing the channel length can result in low performance of the OFF-state current in short-channel devices. The ideal device specifications would be to have the least possible OFF-current (I_{OFF}) and the highest possible ON-current (I_{ON}). This research involves simulating a transistor with a channel length of 10 nm at various dielectric constants. The research begins with a ballistic simulation of the input characteristics of a dual-gated GNR-FET. To know the performance of the device dependency on gate oxide strength, a study is carried out for different gate oxide materials. **Fig. 2** illustrates the transfer characteristics of the GNR-FET under examination for various dielectric constant values (SiO_2=3.9, Si_3N_4=7.5, Al_2O_3=10 and HfO_2=25) in both linear and logarithmic views.

The figure indicates that the GNR-FET device with HfO_2 as a dielectric constant result in a one-order decrease in I_{OFF} and an enhancement of I_{ON}. This improvement in I_{ON} the device's characteristics for higher dielectric values is due to the better electrostatic control of the channel region in GNR-FET with a high-k dielectric material, and simultaneously, the I_{OFF} of the device increases with an increase in dielectric strength at low gate voltages. It is worth mentioning that the values of the I_{ON} and I_{OFF} are established as I_{DS} (V_{DS} = 0.5 V, V_{GS} = 0.6 V) and I_{DS} (V_{DS} = 0.5 V, V_{GS} = 0 V), respectively in this observation. **Fig. 3** shows the variation of ON-current and OFF-current for the GNR channel with different high-k materials, and it is observed from **Fig. 3** that I_{ON} of the GNR-FET increase with high-k dielectrics, whereas I_{OFF} of the device decreases with high-k dielectric. **Fig. 4** depicts the conduction band (CB) profile along the GNR in the ON state of the device. As shown in **Fig. 4**, devices with SiO_2, Si_3N_4, and Al_2O_3 as dielectric materials cover the lower energy path, which leads to lower ON- current compared to devices with HfO_2 as the dielectric material. **Fig. 5** displays the change in transmission probability with energy. It is observed from **Fig. 5** that an increase in the dielectric constant of the material results in a decrease in transmission probability. This decrease in transmission probability results in a decrease in OFF-current.

Therefore, an increase in I_{ON}/I_{OFF} is observed, as shown in **Fig. 3.** The I_{ON}/I_{OFF} ratio comparison for different gate oxide materials is shown in **Fig. 6**. It is observed from **Fig. 6** that I_{ON}/I_{OFF} ratio for GNR-FET is lowest for SiO_2, whereas it is the highest for HfO_2 as the gate dielectric. The observed I_{ON}/I_{OFF} ratio for HfO_2 is 3.8 $\times 10^4$. DIBL is an essential parameter for short channel effects. It is defined as the ratio of the change in threshold voltage (ΔV_T) to the change in drain-source voltage (ΔV_{DS}). The DIBL can be expressed as ΔV_T / ΔV_{DS}. The DIBL plot for various dielectric materials is shown in **Fig. 7**, where it is evident that the DIBL value for SiO_2 dielectric material-based is 174.54 mV/V. In contrast, the DIBL value is reduced to 164.16 mV/V, 62.47 mV/V, and 31.41 mV/V for Si_3N_4, Al_2O_3, and HfO_2 dielectric material-based GNR-FET, respectively. Transconductance (g_m) is a measure of the ability of an electronic device, such as a transistor, to control the current flowing through it by varying the voltage applied to its input terminal. The amplification capabilities of a device can be evaluated based on its Transconductance Gain Factor (TGF). TGF refers to the efficiency with which the drain current is utilized to obtain a desired value of transconductance (g_m). Devices with a higher TGF are more suitable for amplifier designs, particularly for low-power applications. **Fig. 8** shows the g_m and TGF values of devices with different high-k materials as a function of V_{GS}. The results indicate that both g_m and TGF increase for high-k spacer materials due to the gate fringing field-induced inversion charge modulation. The TGF and the charge-based expressions for g_m can be expressed as [40]:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu W}{L}(Q_S - Q_d) \qquad (1)$$

$$\text{TGF} = \frac{g_m}{I_D} \qquad (2)$$

The increase in g_m is directly proportional to the S/D charge difference and μ, as stated in equation (1). In the subthreshold region, the Q_S of the GNR-FET increases gradually due to gate control, while Q_d remains almost constant as the gate fringing field is very low. This leads to a swift increase in subthreshold g_m with V_{GS}. The high-k dielectric material does not significantly enhance Q_S under subthreshold bias, but Q_d slightly decreases due to the increase in reverse drain-to-gate field, resulting in increased g_m. In the superthreshold region, both the gate field and the gate fringing field are strong, causing a significant improvement in both Q_S and Q_d, resulting in almost constant g_m. In addition, the μ is very high under superthreshold bias condition and dominates the g_m. On increasing the high-k material under superthreshold bias, the Q_S remains unaffected while Q_d increases, thereby slightly increasing the g_m. The results in **Fig. 8** also show that the available gain per unit value of power dissipation, TGF=g_m/I_D, improves for higher dielectric material in the subthreshold region.

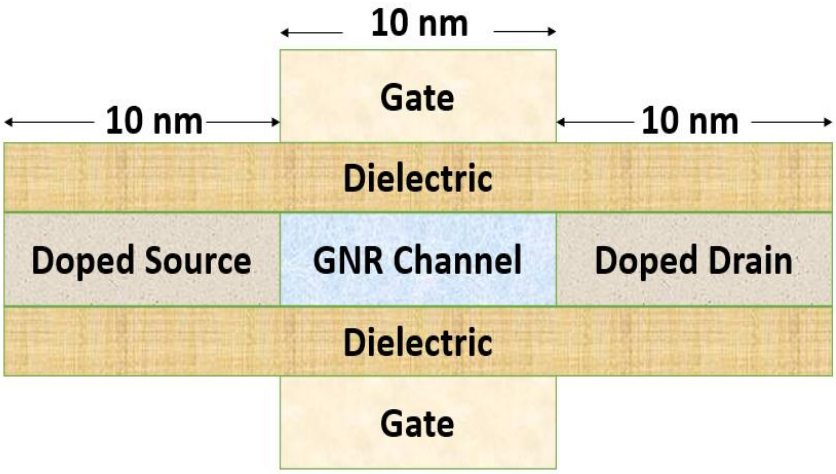

Fig. 1. The simulated device structure.

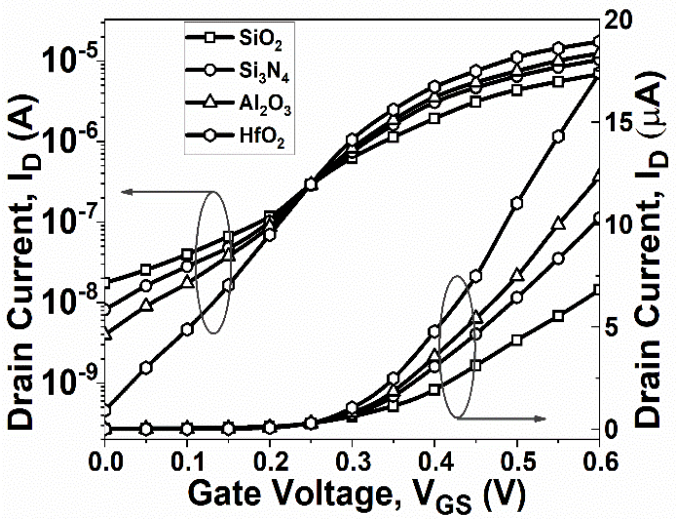

Fig. 2. Transfer characteristics of GNR FETs at V_{DS}= 0.5 V.

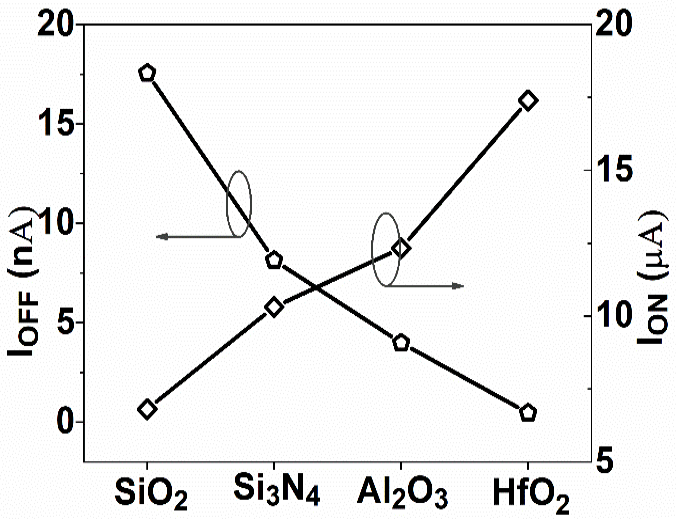

Fig. 3. Variation of ON-current and OFF-current of GNR-FETs with different dielectric materials.

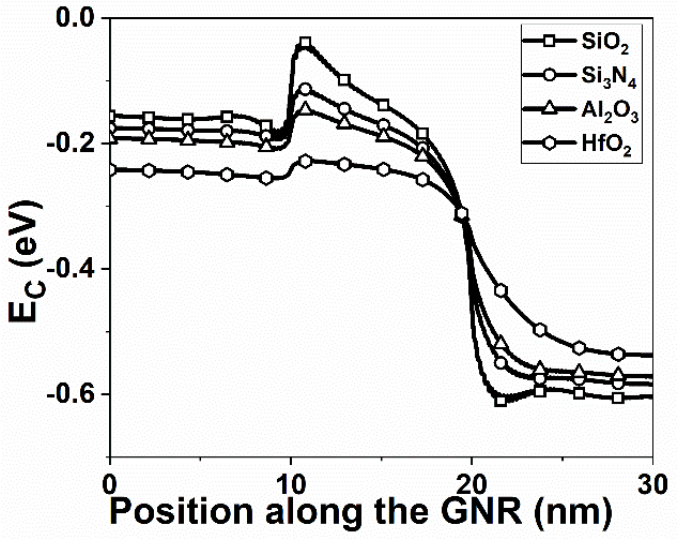

Fig. 4. Conduction band profile of the GNR-FETs at ON-state

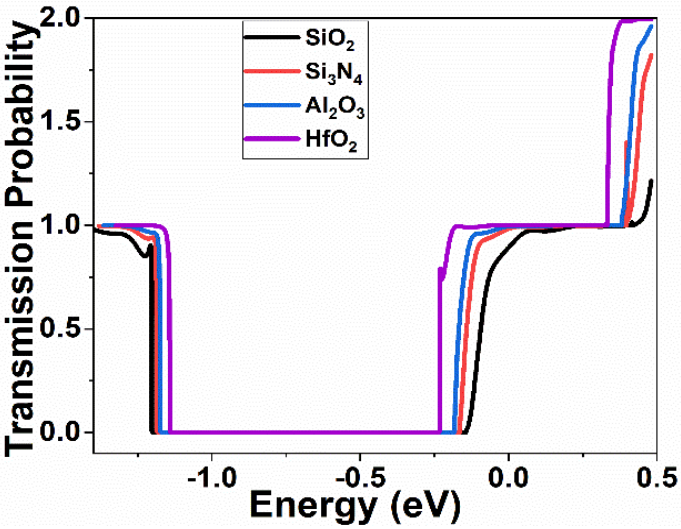

Fig. 5. Variation of transmission probability with energy, E (eV).

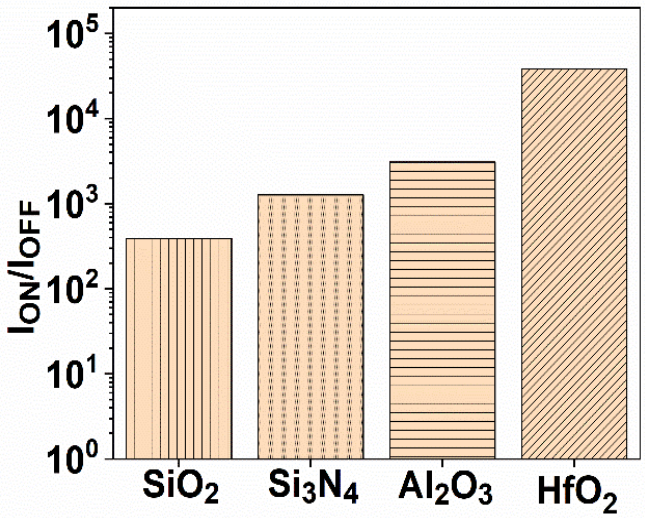

Fig. 6. Variation of current ON/OFF ratio with different dielectric materials.

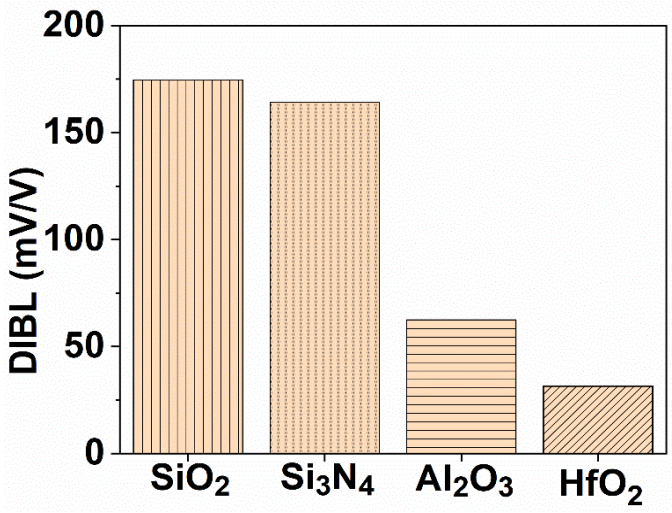

Fig. 7. Variation of DIBL with GNR FETs with different dielectric materials.

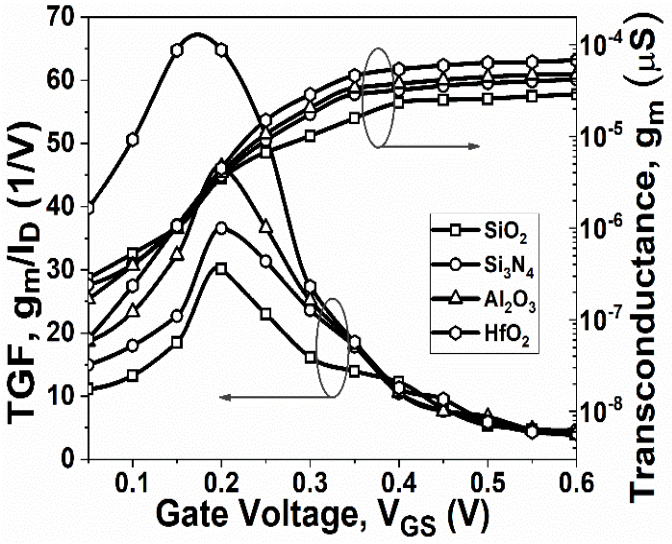

Fig. 8. Variation of g_m and TGF as a function of V_{GS} at V_{DS} = 0.5 V.

This increase in g_m/I_D is due to higher g_m and low I_D resulting from the enhanced drain-to-gate reverse field for high-k material under low-gate bias conditions, as mentioned earlier in the section.

4. Conclusions

The study investigated the impact of dielectric strength on the performance of a GNR-FET. The findings revealed that as the dielectric strength increased, the performance of the GNR-FET ascent, with the drain current and I_{ON}/I_{OFF} ratio increasing while the short channel effect (as indicated by DIBL) increased. The findings also revealed that the analog performance features, such as transconductance and transistor efficiency (TGF) of the GNR-FET are improved with the dielectric strength of the gate oxide material.

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